What is claimed is:

1. A semiconductor memory device comprising:

a memory cell area made up of a plurality of memory cells and having an information bit area which information bits are written in and / or read from and a parity bit area which parity bits are written in and / or read from, and a redundant circuit to replace error bits contained in said information bits and / or said parity bits; and

an error correcting code (ECC) circuit to perform error correcting processing, using a Hamming Code on data including said information bits and said parity bits being written in and /or read from said information bit area or said parity bit area in said memory array; and

wherein a combined use of redundant correcting processing to correct said error bits using a redundant circuit in said memory array with said error correcting processing using said Hamming Code in said ECC circuit is made possible.

2. The semiconductor memory device according to Claim 1, wherein, when reading processing is performed on said information bit area or said parity bit area, said data on which said error correcting processing has been performed is output to only an outside of said memory array without being rewritten into said information bit area or said parity area.

3. The semiconductor memory device according to Claim 1, wherein, when a codeword made up of bits occurs which is beyond a correcting capability of said error correcting processing using

said Hamming Code, said redundant correction processing on said error bits using said redundant circuit is made.

4. The semiconductor memory device according to Claim 1, wherein said error correcting code (ECC) circuit comprises an encoding circuit to output, by arithmetic operations, said parity bit corresponding to said information bit, a decoding circuit to output an error location detecting signal indicating an error bit out of all bits contained in said codeword, and an error correcting circuit to input said error location detecting signal and to output an error bit in a reverse manner.

5. The semiconductor memory device according to Claim 4, wherein said encoding circuit comprises a syndrome tree in which a plurality of AND circuits to which a first test signal is fed is connected to a plurality of exclusive OR circuits in a manner to provide a specified relationship.

6. The semiconductor memory device according to Claim 4, wherein said decoding circuit comprises a syndrome tree in which a plurality of exclusive OR circuits is connected to one another so that a plurality of bits of said information bits and a plurality of bits of said parity bits are input and a plurality of bits of syndromes is output and decoders to which a plurality of NAND circuits to which a plurality of bits of said syndromes is input and in which a plurality of bits of said error location detecting signals are output and a plurality of AND circuits to which a second test signal is fed are connected to one another in a manner to provide a specified relationship.

7. The semiconductor memory device according to Claim 4, wherein, in said error correcting circuit, a plurality of exclusive OR circuits to which a plurality of bits of said error location detecting signals is input together with a plurality of bits of said information bits and a plurality of bits of said parity bits and a plurality of switches to which a third test signal is fed are connected to one another in a manner to provide a specified relationship so that said error bits are output in a reverse manner.

8. A semiconductor memory device according to Claim 1, wherein a memory array comprising said memory cell area and said redundant circuit.

9. A semiconductor memory device comprising:

a memory cell area made up of a plurality of memory cells and having an information bit area which information bits are written in and / or read from and a parity bit area which parity bits are written in and / or read from, and a redundant circuit to replace error bits contained in said information bits and / or said parity bits; and

an error correcting code (ECC) circuit to perform error correcting processing, using a Hamming Code whose cord length is 72 or less on data including said information bits and said parity bits being written in and /or read from said information bit area or said parity bit area in said memory array; and

wherein a combined use of redundant correcting processing to correct said error bits using a redundant circuit in said memory array with said error correcting processing using said Hamming

Code in said ECC circuit is made possible.

10. The semiconductor memory device according to Claim 9, wherein, when reading processing is performed on said information bit area or said parity bit area, said data on which said error correcting processing has been performed is output to only an outside of said memory array without being rewritten into said information bit area or said parity area.

11. The semiconductor memory device according to Claim 9, wherein, when a codeword made up of bits occurs which is beyond a correcting capability of said error correcting processing using said Hamming Code, said redundant correction processing on said error bits using said redundant circuit is made.

12. The semiconductor memory device according to Claim 9, wherein said error correcting code (ECC) circuit comprises an encoding circuit to output, by arithmetic operations, said parity bit corresponding to said information bit, a decoding circuit to output an error location detecting signal indicating an error bit out of all bits contained in said codeword, and an error correcting circuit to input said error location detecting signal and to output an error bit in a reverse manner.

13. The semiconductor memory device according to Claim 12, wherein said encoding circuit comprises a syndrome tree in which a plurality of AND circuits to which a first test signal is fed is connected to a plurality of exclusive OR circuits in a manner to provide a specified relationship.

14. The semiconductor memory device according to Claim 12, wherein said decoding circuit comprises a syndrome tree in which a plurality of exclusive OR circuits is connected to one another so that a plurality of bits of said information bits and a plurality of bits of said parity bits are input and a plurality of bits of syndromes is output and decoders to which a plurality of NAND circuits to which a plurality of bits of said syndromes is input and in which a plurality of bits of said error location detecting signals are output and a plurality of AND circuits to which a second test signal is fed are connected to one another in a manner to provide a specified relationship.

15. The semiconductor memory device according to Claim 12, wherein, in said error correcting circuit, a plurality of exclusive OR circuits to which a plurality of bits of said error location detecting signals is input together with a plurality of bits of said information bits and a plurality of bits of said parity bits and a plurality of switches to which a third test signal is fed are connected to one another in a manner to provide a specified relationship so that said error bits are output in a reverse manner.

16. A semiconductor memory device according to Claim 9, wherein a memory array comprising said memory cell area and said redundant circuit.